Problem 1

Design a circuit that counts the number of 0's present in 4 inputs A, B, C and D. Its output is a multi-bit, representing that count in binary. For example, 0101 has two zeros and therefore the output should be a binary representing 2.

a. Write the truth table for this circuit.

b. Find the minimized logic equations in SOP and POS for each output

c. Draw the corresponding all NAND and all NOR gates logic diagram for this circuit. Label all inputs and outputs.

Problem 2

Design a circuit with inputs A,B,C, and D. Let the two inputs AB represent a two-bit number with A as the high order bit, and CD represent another two-bit number. That is, the values on AB represent four values 00 (0), 01 (1), 10 (2), and 11 (3). The circuit has three outputs: G, E, and L. Output G, E, and L should be 1 only if the number represented by AB is greater, equal, and less than the number represented by CD, respectively.

a. Write the truth table for this circuit.

b. Find the minimized logic equations in SOP and POS for each output

c. Draw the corresponding all NAND and all NOR gates logic diagram for this circuit. Label all inputs and outputs.

Problem 3

Rows and columns of a Karnaugh map are labeled using Gray code. Gary code is a reflective code. One bit Gray code is

0
1

Two bits Gray code is derived by getting the reflection of one bit Gray code

0
1

1
0

And adding 00's about the line and 1's below it:

00
01
11
10

Note that in this code consecutive valuations differ in one variable only. Repeating the process, we can get 3 bit Gray code:

0 00
0 01
0 11
0 10
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1 10
1 11
1 01
1 00

The following table depicts the conversion between four-bit binary and Gray codes.

BCD	Gray
0000	0000
0001	0001
0010	0011
0011	0010
0100	0110
0101	0111
0110	0101
0111	0100
1000	1100
1001	1101
1010	1111
1011	1110
1100	1010
1101	1011
1110	1001
1111	1000

Design a circuit that can convert a BCD code into a Gray.

a. Write the truth table for this circuit.

b. Find the minimized logic equations in SOP and POS for each output

c. Draw the corresponding all NAND and all NOR gates logic diagram for this circuit. Label all inputs and outputs.